For testing, the receiver was mounted in a high speed package and test fixture. The light generated by a high speed 800nm wavelength transmitter was coupled to the detectors using a singlemode fibre. The level of optical power was adjusted by a variable optical postamplifier, a comparator, a decision circuit and an ECL driver. An error rate of $<10^{-6}$ has been demonstrated at 2.4Gbit/s.

In summary, we have fabricated an optoelectronic receiver based on GaAs MESFET technology and a GaAs MSM photodiode. The receiver has an MSM photodiode, a preamplifier, a postamplifier, a comparator, a decision circuit and an ECL driver. An error rate of $<10^{-6}$ has been demonstrated at 2.4Gbit/s.

**References**


AlGaN-GaN heterostructure FETs with offset gate design

R. Gaska, Q. Chen, J. Yang, M. Asif Khan, M.S. Shur, A. Ping and I. Adesida

Indexing terms: Field effect transistors

The DC performance of AlGaN-GaN heterojunction field effect transistors (HFETs) with an offset gate design is reported for the first time. The breakdown voltage for these offset gate devices exhibited a strong dependence on the gate-to-drain separation and the maximum transconductance increased almost linearly with the source-to-gate distance.

The last few years have witnessed strong competition in the development of AlGaN-GaN heterostructure field effect transistors (HFETs), which are considered to be suitable candidates for high power electronics, operating at elevated temperatures and in harsh environments. Transconductances in excess of 200mS/mm, breakdown fields as high as 1.1MV/cm, source-drain currents over 1A/mm, cutoff frequencies of up to 40GHz, and stable DC and microwave performance of devices at temperatures of up to 200°C have been reported recently [1–4]. Rapid progress in the AlGaN-GaN HFET development has been achieved by improving the material and optimising the heterostructure design and doping profiles. In this Letter, we report a further improvement of the AlGaN-GaN HFETs design, achieved by introducing a so-called offset gate (see, for example, [5]).

A palladium stripe was grown by the low pressure metal organic vapour pressure epitaxy and the HFET fabrication procedure were similar to those described previously [6, 7]. Devices with source-to-drain separations $d_{sd} = 2\mu m$ and gate lengths $L = 0.254\mu m$ were studied. The gate offset was introduced in such a way that the ratio of the source-to-gate distance $d_{sg}$ and the gate-to-drain distance $d_{sd}$ varied from 0.2 to 5. These separations, as well as the gate lengths, were determined from the SEM photographs.

The results are presented for two sets of devices (denoted as A and B) from two wafers with different epilayer doping profiles. Both sets of devices have comparable 2D electron Hall mobility at room temperature $\mu (A) = 1220cm^2/Vs$, and $\mu (B) = 1044cm^2/Vs$. Devices from wafer B with higher barrier doping have a more negative threshold voltage (close to $-8V$) and a larger electron sheet concentration $n_s = 1.4 \times 10^{13}cm^{-2}$. Electron sheet concentration for device set A is $n_s = 7 \times 10^{12}cm^{-2}$ and the threshold voltage is close to $-4V$. The gate length of the HFETs on wafer B is 0.25µm; for the devices on wafer A, it varies from 1.3 to 4µm. The transconductances of both sets of devices were $\sim 120-130mS/mm$ with the maximum source-drain currents $> 1A/mm$.

**Fig. 1** Breakdown voltage dependence on gate-to-drain separation for $d_{sd} = 4\mu m$ and gate width of $50\mu m$.

Sample A $V_{th}$ values for gate-to-drain spacings $d_{sd} = 0.5$ and $1.5\mu m$ correspond to gate length $L = 2\mu m$; for $d_{sd} = 1.0$ and $1.5\mu m$, $L = 1\mu m$. Breakdown voltage was measured at gate voltage $V_g = -4V$.

Fig. 1 shows the dependence of the breakdown voltage $V_{th,b}$, on the gate-to-drain separation distance $d_{sd}$. These results were obtained for the HFETs with source-drain openings of 4µm, gate lengths of 1.3 and 2.3µm, and a gate width of 50µm. The breakdown voltage was measured in a sub-threshold regime. As seen from Fig. 1, the breakdown voltage increases with the gate-to-drain distance. The gate-to-drain voltage drops primarily across the depleted region in GaN, which extends beyond the gate into the drain region. The depletion region in GaN, which extends beyond the gate into the drain region.

The depletion region is approximated as a rectangular voltage source with the breakdown field at the drain. Since a high electric field at the drain will lead to the electron injection from the ohmic contact, we expect that the effective breakdown field will be relatively small, since a high electric field at the drain will lead to the electron injection from the ohmic contact. When the depletion region is shorter than the gate-to-source spacing, the breakdown voltage should be determined either by the breakdown field of the GaN channel or by the breakdown field of the AlGaN barrier layer. Hence, the breakdown field should be higher. As can be seen from Fig. 1, the slope of the breakdown voltage dependence on the gate-to-drain spacing $d_{sd}$ increases with $d_{sd}$, and the breakdown field estimated from the largest slope is $\sim 1.3MV/cm$. Similar breakdown fields were recently reported for the HFETs with 1 and 3µm gate-to-drain separations [2, 3].

The breakdown fields close to 1.3MV/cm were obtained in the 50µm wide devices. In wider devices, the breakdown field
intensity was lower. For example, the highest breakdown voltage in the 50μm width device was 170-180V. The 100μm devices with the same values of the gate-to-drain separation and gate length experienced a breakdown at 150-160V. We expect that the breakdown voltage of the AlGaN-GaN HFETs with offset gates can be further increased by improving the metal contacts geometry.

The breakdown voltage $V_{BS}$ is the largest below the threshold voltage ($V_T = V_{PD}$). Above the threshold, the breakdown is 'controllable' and does not lead to destruction of the device. In this regime, $V_{BS}$ decreases almost linearly with the gate voltage. In contrast, in the subthreshold regime, the breakdown in the HFETs leads to surface damage accompanied by surface flashover.[8].

![Fig. 2 Transconductance against gate voltage for Al$_{x}$Ga$_{1-x}$N-GaN HFETs with 50μm width offset gate at source-drain voltage of 10V](image)

We also investigated the effect of the gate offset on the transconductances of the AlGaN-GaN HFETs. The transconductances against gate voltage for 50μm width devices with both 3μm source-to-drain separation and 0.25μm gates are shown in Fig. 2. These measurements were performed at $V_{DS} = 10V$ and the data were obtained for both polarities of the source-drain voltage, which gives the results for two different source-to-gates distances for each device. The data shown in Fig. 2 were obtained for two sets of HFETs with the gates shifted towards one of the contacts (source or drain) by approximately 0.4 and 0.9μm. We can see from the figure that the maximum transconductance increases from 90mS/mm for HFET with source-to-gate separation of 2.25μm to ~120mS/mm for $d_{GO} = 0.5μm$. Devices without the noticeable gate offset exhibited the same transconductance against gate voltage dependencies for both source-drain voltage polarities. The maximum transconductance values for these devices were $g_m = 104-107mS/mm$. Thus, a decrease in the gate-to-source spacing increased the transconductance of the HFETs by >10% in comparison to the devices without the offset gate. This increase is caused by reduced gate-to-source spacing and is related to a decrease in the source series resistance. A further reduction of the source-to-gate separation (beyond 0.5μm) was limited by an increase in the source-to-gate leakage.

We used the transconductance dependence on the source-to-drain distance in order to estimate the maximum increase in the transconductance, which could be achieved by suppressing the source-to-gate leakage and increasing the gate offset (reducing the source-gate distance, $d_{GO}$). The inset in Fig. 2 shows the reciprocal maximum transconductance, $1/g_{m\max}$, against the source-to-gate separation. From the linear approximation of the dependence (solid line in the inset in Fig. 2), we extracted the source resistivity $R_s$ and estimated the $n_s$μ product. The product is ~3 × 10^3 Ω·μ, which is 3.5-4 times smaller than the $n_s$μ values obtained from the Hall measurements in the epilayer structure before the device processing. The intercept with the $1/g_{m\max}$ axis yields the transconductance value of $g_m = 140mS/mm$. From the relationship between external and internal transconductances we find:

$$\frac{1}{g_m} = \frac{1}{g_m\max} + R_s$$

(1)

where

$$R_s = R_c + R_h$$

Here, $R_c$ is source contact resistance, and $R_h$ is the resistance of the 2D channel between the source and the gate. $R_c$ is proportional to the source-gate separation and vanishes when $d_{GO} \rightarrow 0$. Thus, the transconductance $g_{m\max} = g_m(1+R_h/R_s)$. The comparison $g_{m\max}$ and $g_m$ for the HFET without the gate offset yields the maximum enhancement of transconductance achievable in our devices by introducing an offset gate design. We estimate that this enhancement could be as high as 30%. The source contact resistance $R_c$ determined from the TLM measurements, was 2.5Ωmm.

We also investigated the effect of the gate offset on the transconductance of the AlGaN-GaN HFETs. The devices with offset gates exhibited lower gate-to-drain leakage currents and higher breakdown voltages. We observed more than a 10% increase in the transconductance compared with devices without the offset gate. We expect that the transconductance can be further increased by reducing the source resistance, and that the gate offset can be further increased (source-to-gate separation decreased) if the source-to-gate leakage is suppressed.

Acknowledgment: The work at APA Optics, Inc. and RPI has been supported by the Office of Naval Research under contract No. N00014-97-C-0033 (Project Monitor Dr. Colin Wood).

References


1256 ELECTRONICS LETTERS 3rd July 1997 Vol. 33 No. 14
Avalanche noise in submicrometre pin diodes

D.C. Herbert

Indexing terms: pin diodes, Semiconductor device noise

It is shown that recent measurements of noise suppression in thin GaAs pin diodes by Hu et al. can be explained as a dead space phenomenon and are consistent with the $\alpha/\beta$ ratio approaching unity at high electric fields.

Introduction: Recent measurements of avalanche noise by Hu et al. [1] showed that for a series of GaAs pin diodes with increasing $\gamma$ region width, the excess noise factor was greatly reduced when compared with the values expected from the classical McIntyre model. This was attributed to the excess noise factor being greatly reduced when compared with the values expected from the classical McIntyre model. The ratio of electron and hole ionisation coefficients $\alpha/\beta$ increases for increasing electric field in the thin diodes. This is contrary to results obtained from multiplication data which show $\alpha/\beta$ approaching unity at high electric fields [4]. This interpretation also implies that the noise suppression may be material specific. The observation of noise suppression has important implications for high speed avalanche devices (APD and IMPATT) and in this Letter, we show that the suppression is a general phenomenon related to dead space and is consistent with the $\alpha/\beta$ ratio approaching unity in GaAs at high fields.

Theory: We use the semi-analytical trajectory method to solve the hot carrier Boltzmann equation, and a modified Keldysh form for the ionisation scattering rates [5]. The device is divided into a set of regions where a region is defined as the distance over which the potential drops by 2kT (~52meV). Analytical solutions of the Boltzmann equation are constructed within each region and these solutions are matched at the region boundaries. To study the noise, a sequence of solutions is generated in which a particle originates in one region and the corresponding ionisation probability is determined by a set of ionisation trajectories $\alpha_j(x, F(x))$, $\beta_j(x, F(x))$, where $n$ labels the region of origin and $\alpha$, $\beta$ refer to electrons and holes respectively [6]. $\alpha_j$, $\beta_j$ are obtained by solving the Boltzmann equation for unit current with no allowance for energy loss in the ionising collisions. These ionisation coefficients only describe one ionisation event along the trajectory and therefore differ from the conventional definition, showing no ionisation overshoot. After an ionisation event, the particles switch to new $\alpha_j$, $\beta_j$ trajectories which are determined by both the position and the computed residual kinetic energy.

After obtaining a full set of $\alpha_j$, $\beta_j$, random numbers are used with these probabilities to determine the positions and times of ionisation events for a particle initiating at a given position. The particles are assumed to move at the saturated drift velocity and each generated particle is started in turn with an average initial kinetic energy, which determines the extent of the particles dead space. The procedure continues until all particles have left the diode. The excess noise factor is then computed from the expression

$$F = \frac{\langle M^2 \rangle}{\langle M \rangle^2}$$

where $M$ is the multiplication obtained from a single trial and the averaging is performed over 10$^4$ trials.

Results: In Fig. 1, we show the computed excess noise for a sequence of GaAs pin diodes with varying $\gamma$ region width and compare with the experimental values of Hu et al. for the 0.8 and 0.15um diodes. The phonon scattering rates were adjusted slightly to achieve agreement with the 0.8um data and this had the effect of reducing the $\alpha/\beta$ ratio from the value of 1.65, obtained by Bullman et al. [8], to 1.51. The theoretical energy relaxing path lengths $\gamma$ are shown in Fig. 2. The theoretical noise values for the 0.5um diode are close to the values for the 0.8um diode, suggesting that the noise suppression mechanism sets in at ~0.5um. The experimental data of Hu et al. is fairly uniformly spaced for the set of diodes between 0.1 and 0.5um and deviates in detail from the theoretical values. It would be helpful to have more data to check these findings.

![Fig. 1 Theoretical excess noise factors for GaAs pin diodes with $\gamma$ region width $w$ varying from 500 to 8000Å.
Experimental values for comparison taken from Hu et al. Studies assumed pure electron injection.
\[ w = 500 \]
\[ w = 2000 \]
\[ w = 1000 \]
\[ w = 500 \]
\[ \text{Exp} w = 8000 \]

Fig. 1 Theory and hole energy relaxing path lengths for GaAs.
These are obtained by cancelling stimulated emission with phonon absorption and use saturated drift velocity at high energy as described by Herbert [6]. Average distance required in field direction for the particle to lose 2kT of energy is $\gamma$. Herbert [5] described model for phonon scattering at high kinetic energy.

The suppression of noise can be understood as a dead space phenomenon. In very thin diodes, the dead space can extend through a large fraction of the $\gamma$ region, and it becomes possible for the $\gamma$ region width to be smaller than two dead spaces. In this case the $\gamma$ region can extend through a large fraction of the $\gamma$ region, and it becomes possible for the $\gamma$ region width to be smaller than two dead spaces. In this case it is only possible for the initiating particle to ionise once before leaving the diode, and fluctuations involving high multiplication events are strongly suppressed, causing the reduction in excess noise.